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IN THE SPECIFICATION:

(1) The paragraph from page 1, line 3 to page 1, line 3 has been amended as follows:

SEMICONDUCTOR TEST APPARATUS FOR TESTING SEMICONDUCTOR DEVICE THAT PRODUCES OUTPUT DATA BY ITS INTERNAL CLOCK TIMING

(2) The paragraph from page 1, line 26 to page 1, line 30 has been amended as follows:

This type of semiconductor test apparatus will now be described with reference to ~~FIG. 8~~ FIG. 7. This drawing is a block diagram showing a schematic structure of a conventional general semiconductor test apparatus (LSI tester).

(3) The paragraph from page 2, line 10 to page 2, line 19 has been amended as follows:

In the conventional semiconductor test apparatus having such a structure, a predetermined test pattern signal is first input to the device under test 101 from a non-illustrated pattern generator, and a ~~predetermined~~ resultant signal is output as output data from the device under test 101. The output data output from the device under test 101 is input to the level comparator 111. The output that is input to the level comparator 111 is compared with a comparison voltage in level, and output to the flip-flop 121.

(4) The paragraph from page 3, line 2 to page 3, line 16 has been amended as follows:

As described above, in the conventional semiconductor test apparatus (LSI tester), the output data output from the device under test is acquired with a timing of a strobe output with a timing preset in the tester, and this strobe is used as a timing signal output from the timing generator provided independently from the device under test. However, in the conventional semiconductor test apparatus which acquires output data of the device under test by using the independent timing signal output from the tester in this manner, there ~~occurs~~ arises a problem that, for a device having a function for generating an internal clock faster than a system clock ~~is generated in the device and~~, it is impossible to ~~cope with the test of~~ test such a high-speed device which outputs output data with a timing of this internal clock.

(5) The paragraph from page 3, line 17 to page 4, line 8 has been amended as follows:

In recent years, the progress in ~~an increase of~~ increasing a speed of LSIs is significant, and a new semiconductor device as typified by, e.g., an ODR (Octal Data Rate) type device is ~~provided~~ introduced in order to increase a speed of data transfer. In this type of device, as shown in FIG. 9, an internal clock having a frequency which is n-fold of that of a system clock of a device 101 is generated by a PLL circuit or the like, and data is output with a timing of the internal clock which is faster than the system clock. For

example, in the ODR type device, the internal clock which is fourfold of the system clock is generated, and data is output at a DDR (Double Data Rate) in synchronization with both edges, i.e., a rise edge and a fall edge of this internal clock. As a result, data output at a data rate which is eightfold of that of the system clock is realized. The DDR is a mode which performs data transfer with both timings of the rise edge and the fall edge of each internal clock signal, and enables double data transfer with the same clock cycle as compared with an SDR (Single Data Rate) mode which performs data transfer only at the rise edge (or the fall edge) of the internal clock.

(6) The paragraph from page 4, line 29 to page 5, line 11 has been amended as follows:

The present invention is proposed in order to solve such a problem in the prior art, and it is an object of the present invention to provide a semiconductor test apparatus which enables a test of a device under test which outputs data with edge timings of a system clock and at a data rate of an internal clock faster than ~~a~~ the system clock, e.g., a high-speed device as typified by an ODR (Octal Data Rate) type device by acquiring a system clock output from the device under test, and ~~acquiring~~ producing a recovery clock having a frequency of an internal clock faster than the system clock

with a rise edge timing or a fall edge timing of the system clock.

(7) The paragraph from page 5, line 14 to page 6, line 7 has been amended as follows:

To achieve this aim, ~~as described in claim 1,~~ a semiconductor test apparatus according to the present invention comprises a first time interpolator which receives a clock output from a device under test, acquires the clock by using a plurality of strobes having specified timing intervals, outputs the clock as time-series level data, selectively receives level data indicative of an edge timing of a rise edge and/or a fall edge of the level data, and outputs positional data indicative of an edge timing of the selected level data; a second time interpolator which receives output data output from the device under test, acquires the output data by using a plurality of strobes having specified timing intervals, and outputs the output data as time-series level data; a digital filter which receives and holds <u>the</u> positional data output from the first time interpolator, and outputs a recovery clock indicative of a predetermined edge timing from one or more sets of the positional data; and a data selection circuit which receives the time-series level data output from the second time interpolator, selects the level data with an edge timing of the recovery clock output

from the digital filter, and outputs the level data as measurement data of the device under test.

(8) The paragraph from page 7, line 13 to page 7, line 24 has been amended as follows:

Level data and positional data indicative of an edge timing of a clock can be acquired by the first timer interpolator. However, for example, when the device under test outputs data in accordance with an internal clock having a frequency which is n-fold of that of a system clock, only one rise edge or fall edge can be detected in n cycles ~~even if~~ of the internal clock when an edge timing of the system clock having a 1/n frequency is obtained, and a signal change point (a rise edge or a fall edge) cannot be detected in any other cycle. As a result, the timing edge of ~~an~~ the internal clock having an n-fold frequency can be detected for only once in n cycles.

(9) The paragraph from page 8, line 30 to page 10, line 4 has been amended as follows:

Specifically, ~~as described in claim 2,~~ the first time interpolator comprises: a plurality of sequence circuits which receive clocks output from the device under test and which are connected with each other in parallel; a delay circuit which sequentially inputs strobes delayed at specified timing intervals to the plurality of sequence circuits, and outputs time-series level data from the sequence circuits; an edge

selector which selectively outputs level data indicative of a rise edge of the time-series level data output from the plurality of sequence circuits, level data indicative of a fall edge of the same, or level data indicative of the rise edge and the fall edge of the same; and an encoder which receives the level data selected by the edge selector, encodes it into positional data indicative of an edge timing and outputs it, the digital filter comprises one or more registers which are connected with each other in series, sequentially store positional data output from the first time interpolator and output the stored positional data with a predetermined timing, and outputs a recovery clock indicative of a predetermined edge timing from one or more sets of positional data output from the registers, the second time interpolator comprises a plurality of sequence circuits connected with each other in parallel which receive output data output from the device under test; and a delay circuit which sequentially inputs strobes delayed at specified timing intervals to the plurality of sequence circuits and outputs time-series level data from the sequence circuits, and the data selection circuit comprises a selector which selects one set of data in the time-series level data input from the second time interpolator with the recovery clock output from the digital filter being used as a selection signal and outputs it as measurement data of the device under test.

(10) The paragraph from page 10, line 5 to page 10, line 15 has been amended as follows:

Moreover, ~~as described in claim 3,~~ the edge selector comprises one or more selector circuits each of which includes: a first AND circuit which receives a reverse output of one sequence circuit and a non-reverse output of a sequence circuit on a next stage; a second AND circuit which receives a non-reverse output of one sequence circuit and a reverse output of a sequence circuit on a next stage; an OR circuit which receives outputs from the first and second AND circuits; and a selector which selects one of outputs from the first AND circuit, the second AND circuit and the OR circuit.

(11) The paragraph from page 10, line 16 to page 10, line 27 has been amended as follows:

According to the semiconductor test apparatus of the present invention having the above-described structure, the first and second time interpolators including the edge selector, digital filter and the data selection circuit can be easily constituted by using existing means such as the sequence circuits, the delay circuit, the encoder, the registers, the selector, the AND circuits, the OR circuit or the like. As a result, the semiconductor test apparatus according to the present invention can be realized by using a simple structure without ~~a~~ complication, ~~an~~ increase in size, ~~an~~ increase in cost and others of an LSI tester.

(12) The paragraph from page 11, line 23 to page 11, line 30 has been amended as follows:

Further, ~~as described in claim 4,~~ the semiconductor test apparatus according to the present invention has a structure in which the digital filter comprises an edge detection circuit which detects presence/absence of an edge of the positional data input from the first time interpolator, and outputs the positional data stored in the registers when the edge is detected.

(13) The paragraph from page 12, line 9 to page 12, line 16 has been amended as follows:

For example, in case of a system clock of an ODR type device, its data rate is 1/8 of a ~~date~~ data rate of the output data. Therefore, when only the ~~only~~ positional data of the rise or fall edge of the system clock acquired by the first interpolator is used, a signal change point (a rise edge and a fall edge) is detected once in eight rise and fall edges of the output data, and the output data output at an eightfold data rate cannot be acquired.

(14) The paragraph from page 13, line 6 to page 13, line 11 has been amended as follows:

Moreover, ~~as described in claim 5,~~ the registers of the digital filter are configured to output the positional data stored therein with a predetermined timing irrespective of

presence/absence of the edge of the positional data detected by the edge detection circuit.

(15) The paragraph from page 13, line 21 to page 14, line 8 has been amended as follows:

~~Of~~ Out of the positional data of the clock output from the first time interpolator, only the ~~only~~ positional data whose edge is detected can be stored in the registers and used as a reference of the recovery clock ~~like claim 4 mentioned above~~. However, when the edge of the positional data is not detected due to an ~~affect~~ influence of, e.g., jitters, a quantity of positional data to be acquired is small or a cycle in which positional data can be acquired cannot be set fixed in some cases. Therefore, when obtaining an average value of a plurality of sets of positional data and outputting the recovery clock, many registers must be provided in order to output the accurate recovery clock. Thus, in the present invention, when the edge of the positional data to be acquired is not detected, the positional data which has been already stored in a previous cycle and whose edge is detected is output from the registers, and the recovery clock can be output based on this positional data.

(16) The paragraph from page 14, line 9 to page 14, line 15 has been amended as follows:

As a result, a positional data acquisition cycle can be set fixed while reflecting an edge timing of the actually

acquired positional data, the number of registers to be set can be optimized, and the reliable semiconductor test apparatus with a simple structure can be realized without ~~a~~ complication, ~~an~~ increase in size, ~~an~~ increase in cost and others of the test structure.

(17) The paragraph from page 15, line 2 to page 15, line 8 has been amended as follows:

Moreover, ~~as described in claim 6,~~ when two or more registers are provided, the digital filter comprises an average value calculation circuit which receives positional data output from each of the two or more registers, calculates an average value of edge timings indicated by respective sets of positional data, and outputs the average value as the recovery clock.

(18) The paragraph from page 15, line 28 to page 16, line 3 has been amended as follows:

Additionally, ~~as described in claim 7,~~ the digital filter comprises an average value changeover switch which selects one of the positional data output from one register among the two or more registers and the average value output from the average value calculation circuit, and outputs it as the recovery clock.

(19) The paragraph from page 16, line 25 to page 16, line 30 has been amended as follows:

Further, ~~as described in claim 8,~~ the digital filter comprises a timing correction circuit which adds a predetermined correction value to the positional data output from the registers, corrects the edge timing indicative of the positional data, and outputs a result as the recovery clock.

(20) The paragraph from page 17, line 25 to page 18, line 1 has been amended as follows:

Furthermore, ~~as described in claim 9,~~ the semiconductor test apparatus according to the present invention comprises a jitter detection circuit which receives a plurality of recovery clocks output from the digital filter, detects a phase difference between edge timings indicated by the respective recovery clocks and obtains a jitter of the clock of the device under test.

(21) The paragraph from page 18, line 2 to page 18, line 17 has been amended as follows:

According to the semiconductor test apparatus of the present invention having such a structure, by providing the jitter detection circuit which receives the plurality of recovery clocks, a phase difference between the ~~recover~~ <u>recovery</u> clocks can be detected by applying subtraction processing to the positional data indicative of the edge timings of the respective recovery clocks. Moreover, ~~a~~ distribution of this phase difference can be obtained, and it can be output as distribution data showing irregularities or

spread of the phase ~~difference~~ differences. The phase difference between the recovery clocks represents a jitter of the system clock of the device under test, and it is possible to perform jitter analysis of the clock and the output data of the device under test by obtaining the phase difference between the recovery clocks and its distribution data.

(22) The paragraph from page 18, line 26 to page 19, line 1 has been amended as follows:

Additionally, ~~as described in claim 10,~~ the semiconductor test apparatus according to the present invention comprises a bus which connects the first and second time interpolators with each other, and distributes data output from the first and second time interpolators to a predetermined data selection circuit.

(23) The paragraph from page 20, line 3 to page 20, line 20 has been amended as follows:

FIGS. ~~5~~ 5(a) and 5(b) are signal diagrams in case of acquiring output data with an edge timing of a system clock when a mode changeover switch of a digital filter is changed over to Direct Edge, in which FIG. 5(a) shows an example of acquiring data at a rise edge of an edge timing of a clock, and FIG. 5(b) shows an example of acquiring data at both of a rise edge and a fall edge of the same;

FIGS. ~~6~~ 6(a) and 6(b) are signal diagrams showing an example of acquiring a recovery clock with rise and fall edge

timings of a system clock in the digital filter by changing a mode of the edge selector to SDR: Rise Edge;

FIG. 7 is a block diagram showing a ~~structure of a semiconductor test apparatus according to a second embodiment of the present invention~~ schematic structure of a conventional semiconductor test apparatus;

FIG. 8 is a block diagram showing a ~~schematic structure of a conventional general semiconductor test apparatus~~ structure of a semiconductor test apparatus according to a second embodiment of the present invention;; and

(24) The paragraph from page 21, line 5 to page 21, line 15 has been amended as follows:

FIG. 1 is a block diagram showing a structure of a semiconductor test apparatus according to ~~a~~ the first embodiment of the present invention. As shown in the drawing, the semiconductor test apparatus according to this embodiment comprises an LSI tester 10 which conducts a function test of a device under test (DUT) ~~1,~~. ~~the~~ The LSI tester 10 acquires output data output from the device under test 1 as measurement data, and judges the acceptability of the device under test 1 ~~is judged~~ by comparing the measurement data with predetermined expectation value data.

(25) The paragraph from page 22, line 14 to page 22, line 21 has been amended as follows:

The LSI tester 10 fetches a recovery clock indicative of an adequate edge timing with a desired frequency from a system clock of the device under test 1 by inputting ~~a~~ the system clock and output data output from the device under test 1 to each channel (each source synchronous circuit), and acquires output data with a timing indicated by the recovery clock, thereby outputting it as measurement data.

(26) The paragraph from page 24, line 23 to page 24, line 29 has been amended as follows:

The plurality of flip-flops 21a to 21n are composed of D type flip-flop groups connected with each other in parallel in this embodiment, and each flip-flop receives an output signal (clock or output data) output from the device under test through the level comparator 11 as input data. Moreover, ~~it~~ each flip-flop outputs the received data ~~input~~ with a predetermined timing by using the strobe input through the delay circuit 22 as a clock signal.

(27) The paragraph from page 26, line 5 to page 26, line 25 has been amended as follows:

Further, the strobes input to the flip-flops 21a to 21n can be set to an arbitrary timing and frequency, and different input timings or delay quantities can be set depending on the clock side and the output data side. In this embodiment, by providing a timing generator or the like in accordance with each of the channels 10a to 10n of the source synchronous

circuits, the strobes can be independently input depending on the clock side and the output data side (see STRB shown in FIG. 1). As a result, it is possible to adjust the strobes to an appropriate timing in accordance with a phase difference of the clock and the output data output from the device under test 1. The clock and the output data output from the device under test 1 do not always necessarily match with each other in phase and, for example, a setup time may be ~~minus or plus~~ added to or subtracted from one another in some cases. Therefore, in such a case, by changing the timing of the strobes depending on the clock side and the output data side, it is possible to adjust the strobes to be output with an appropriate timing to the clock and the output data having a phase difference.

(28) The paragraph from page 27, line 1 to page 27, line 6 has been amended as follows:

Specifically, the edge selector 23 in this embodiment comprises a plurality of selector circuit groups each including two AND circuits 24 and 25, one OR circuit 26 and one selector 27 ~~in accordance with~~ for each of the outputs of the flip-flops 21a to 21n.

(29) The paragraph from page 29, line 4 to page 29, line 12 has been amended as follows:

The encoder 28 is configured to receive time-series level data output from the plurality of selectors 27a to 27b of the

edge selector 23, encode the level data and output ~~it~~ the encoded result. Specifically, data sequentially output from the flip-flops 21a to 21n at fixed intervals are sequentially input to the encoder 28 through the respective selectors 27a to 27n of the edge selector 23, encoding is carried out with a timing at which all sets of data are provided, and its result is output.

(30) The paragraph from page 30, line 26 to page 31, line 4 has been amended as follows:

Moreover, the time-series level data output from the flip-flops ~~21a~~ 21b to 21n on the output data side are directly input to the selector 30 on the output side as input data without interposing the edge selector 23 and the encoder 28, and the recovery clock acquired by the digital filter 40 on the clock side or the positional data acquired by the encoder 28 on the clock side is selectively input as a selection signal by a control of the time interpolator bus 50.

(31) The paragraph from page 31, line 5 to page 31, line 10 has been amended as follows:

As a result, in the selector 30 on the output data side, one set of data in the time-series level data output from the flip-flops 21a to 21n of the output data side time interpolator 20 is selected ~~with~~ by a selection signal which is either the recovery clock from the digital filter 40 or the

positional data from the encoder 28 ~~being used as a selection signal~~.

(32) The paragraph from page 31, line 19 to page 31, line 28 has been amended as follows:

On the other hand, the time-series level data output from the flip-flops ~~21a~~ 21b to 21n on the clock side is directly input to the selector 30 on the clock side as input data without interposing the edge selector 23 and the encoder 28, and the positional data acquired by the encoder 28 on the clock side or the recovery clock acquired by the digital filter 40 on the clock side is selectively input as a selection signal by a control of the mode changeover switch 47 of the above-described digital filter 40.

(33) The paragraph from page 33, line 16 to page 33, line 27 has been amended as follows:

The digital filter 40 is provided to the source synchronous circuit 10a on the clock side, and it receives and holds positional data of the clock output from the encoder 28 of the time interpolator 20 on the clock side and outputs a recovery clock indicative of a predetermined edge timing from one or more sets of positional data. Specifically, the digital filter 40 comprises a plurality of registers 41 (41a to 41n), an edge detection circuit 42, an edge changeover switch 43, an average value calculation circuit 44, an average

value changeover switch 45, a timing correction circuit 46 and a mode changeover switch 47.

(34) The paragraph from page 34, line 10 to page 34, line 18 has been amended as follows:

More specifically, as to the registers 41a to 41n, the positional data of the encoder 28 is first input and stored to the register 41a on the forefront state, and this positional data is output with a predetermined timing and sequentially input to the registers 41b to 41n on the next stage which are connected with each other in series. The positional data output from the register ~~n~~ 41n on the last stage is input to the later-described average value calculation circuit 44.

(35) The paragraph from page 35, line 21 to page 35, line 28 has been amended as follows:

The edge detection circuit 42 detects presence/absence of an edge of the positional data input from the encoder 28 of the time interpolator 20. Moreover, when the edge is detected, this ~~circuits~~ circuit stores the positional data from which the edge is detected in the register 41a on the forefront stage, and outputs the positional data which has been already stored in each of the registers 41a to 41n.

(36) The paragraph from page 36, line 19 to page 37, line 5 has been amended as follows:

Specifically, the edge detection circuit 42 receives the positional data from the encoder 28, and detects

presence/absence of an edge in this positional data. Moreover, when an edge of the positional data is detected, an enable signal is output to the register 41a on the forefront stage ("E" shown in FIG. 1), and the register 41a on the forefront stage is ~~caused to enter~~ changed to a data input enabled state. As a result, the positional data from which the edge is detected is stored in the register 41a on the forefront stage. On the other hand, when the edge of the positional data is not detected, the edge detection circuit 42 does not output the enable signal. Therefore, when the edge of the positional data is not detected, the register 41a on the forefront stage ~~enters~~ is changed to an input disabled state, and the positional data from which the edge is not detected is not stored in the register 41a.

(37) The paragraph from page 37, line 13 to page 37, line 22 has been amended as follows:

As a result, out of the positional data acquired by the time interpolator 20, only the ~~only~~ positional data from which the edge indicative of a signal change point is detected is stored in the registers 41a to 41n as positional data which can be a reference of the recovery clock, and output. Additionally, when ~~the~~ an edge of the positional data is not detected in the current cycle, ~~the~~ an edge of the positional data is detected in subsequent cycles, and the positional data stored in each of the registers 41a and 41n is output.

(38) The paragraph from page 38, line 9 to page 38, line 15 has been amended as follows:

The edge changeover switch 43 is switching means which is connected with the edge detection circuit 42 and selectively switches between the trigger signal which is input to each of the registers 41a to 41n through the pulser 42a of the edge detection circuit 42 and the strobe which is output from the delay circuit 22 of the time interpolator 20.

(39) The paragraph from page 39, line 1 to page 39, line 9 has been amended as follows:

Specifically, the edge changeover switch 43 switches a mode to input the trigger signal which is output from the pulser 42a of the above-described edge detection circuit 42 as a timing signal (trigger signal) which is used to output the positional data stored in the registers 41a to 41n ((1) Edge Sync Mode shown in FIG. 2), and a mode to input the strobe which is output from the delay circuit 22 of the time interpolator 20 ((2) ~~Continuously~~ Continuous Mode shown in ~~the same drawing~~ FIG. 2).

(40) The paragraph from page 39, line 10 to page 39, line 17 has been amended as follows:

Furthermore, by switching this edge changeover switch 43 and selecting the strobe of the delay circuit 22 ((2) ~~Continuously~~ Continuous Mode), a strobe signal which is output from the delay circuit 22 of the time interpolator 20 with a

predetermined timing can be input to the registers 41a to 41n, and the positional data can be output from each of the registers 41a to 41n irrespective of presence/absence of edge detection.

(41) The paragraph from page 39, line 18 to page 40, line 6 has been amended as follows:

In this (2) ~~Continuously~~ Continuous Mode, since the enable signal is not input to the register 41a on the forefront stage, the positional data stored in the register 41a is held as it is, and the positional data which is output from the registers 41a to 41n-1 on the previously stage is stored in the registers 41b to 41n on the next and subsequent stages. Therefore, when the edge of the positional data is detected, the respective registers 41a to 41n sequentially store and output the positional data thereof like the example of the above-described edge detection circuit 42. When the edge of the positional data is not detected, the already stored positional data in the previous cycle is sequentially output and stored in the registers on the next stage. As a result, in this (2) ~~Continuously~~ Continuous Mode, the positional data indicative of the edge timing is sequentially output with a timing of the strobe of the delay circuit 22 irrespective of presence/absence of edge detection of the positional data.

(42) The paragraph from page 40, line 7 to page 40, line 26 has been amended as follows:

As described above, in this embodiment, by providing the edge changeover switch 43, when the edge of the positional data from the time interpolator 20 is not detected, it is possible to select either disabling the output of the positional data from the register 41 which can be a reference of the recovery clock ((1) Edge Sync Mode) or enabling the output of the positional data in the previous cycle stored in the register ((2) ~~Continuously~~ Continuous Mode). As a result, it is possible to selectively adopt the positional data in accordance with a test content or the like. For example, the only positional data from which the edge is detected is selected in case of performing a further precise function test or jitter analysis or the like only by using an actual edge timing of the system clock of the device under test ((1) Edge Sync Mode), and the already stored positional data in the previous cycle is also used in case of conducting a logic test which checks output data or clock data of the device under test from an average value with a fixed cycle ((2) ~~Continuously~~ Continuous Mode).

(43) The paragraph from page 41, line 20 to page 41, line 24 has been amended as follows:

The average value changeover switch 45 selects one of the average value which is output from the average value

calculation circuit 44 and the positional data which is output from one of the plurality of registers 41, and outputs ~~it~~ the selected value as a recovery clock.

(44) The paragraph from page 43, line 25 to page 44, line 7 has been amended as follows:

For example, when the clock of the device under test 1 is obtained by using the strobe composed of eight bits, the set value can be set as a value which shifts an edge timing of the positional data by an arbitrary bit number within a range of the eight-bit strobe. Specifically, "0", "+1", "-2" or the like can be set as the set value, and it is possible to correct, e.g., delay the edge timing of the positional data by one bit or ~~hasten~~ advance the same by two bits in the ~~rage~~ range of, e.g., an eight-bit strobe based on such a set value. As a result, the setup time or the hold time of the output data can be taken into consideration, and the recovery clock corrected to have an adequate edge timing can be output.

(45) The paragraph from page 44, line 20 to page 45, line 5 has been amended as follows:

Specifically, in this embodiment, the mode changeover switch 47 can be selectively connected with the output side of the encoder 28 on the clock side and the output side of the timing correction circuit 46 of the digital filter 40, and can switch between obtaining the positional data of the encoder 28 ((1) Direct Edge shown in FIG. 1) and obtaining ~~a~~ the recovery

clock acquired by the digital filter 40 ((2) Hold Edge shown in the same drawing). By switching ~~of~~ this mode changeover switch 47, (1) Direct Edge can be selected in case of a device which outputs output data with a timing of the system clock of the device like a regular SDR type device, and (2) Hold Edge can be selected in case of testing the device which outputs output data at a data rate of an internal clock faster than the system clock of the device like an ODR type device.

(46) The paragraph from page 46, line 15 to page 46, line 19 has been amended as follows:

Incidentally, although not shown in FIG. 1, the plurality of time interpolator ~~bus~~ <u>buses</u> 50 which distribute data to the plurality of source synchronous circuits are provided in accordance with the respective source synchronous circuits (respective channels).

(47) The paragraph from page 47, line 30 to page 48, line 5 has been amended as follows:

First, when a predetermined test pattern signal is input to the device under test 1 from a non-illustrated pattern generator provided to the test apparatus, a predetermined clock (system clock) and output data corresponding to ~~a~~ <u>the test</u> pattern signal are output from the device under test 1.

(48) The paragraph from page 48, line 10 to page 48, line 13 has been amended as follows:

The clock and the output data input to each synchronous circuit are input to the level comparator 11, compared with a comparison voltage in level, and then input to each ~~timer~~ time interpolator 20.

(49) The paragraph from page 49, line 28 to page 50, line 8 has been amended as follows:

First, the positional data is input to the edge detection circuit 42, and presence/absence of an edge is detected. At this time, ~~there is selected~~ one mode is selected to input an enable signal output from the edge detection circuit 42 ((1) Edge Sync Mode shown in FIG. 2) or to input a strobe signal output from the delay circuit 22 of the time interpolator 20 ((2) Continuously Mode shown in the same drawing) by switching ~~of~~ the edge changeover switch 43 as a timing signal (trigger signal) which is used to output the positional data stored in the registers 41a to 41n.

(50) The paragraph from page 50, line 22 to page 51, line 1 has been amended as follows:

As a result, out of the positional data obtained by the time interpolator 20, only the ~~only~~ positional data from which the edge indicative of a signal change point is detected is sequentially stored in and output ~~to~~ from the registers 41a to 41n as positional data which can be a reference of the recovery clock. When the edge of the positional data is not detected in the current cycle, the positional data that has

been stored in each of the registers 41a to 41n is output by detection of the edge of the positional data in subsequent cycles.

(51) The paragraph from page 51, line 2 to page 51, line 6 has been amended as follows:

On the other hand, when (2) ~~Continuously~~ Continuous Mode is selected, ~~a~~ the strobe signal is input to the registers 41a to 41n from the delay circuit 22 of the time interpolator 20 irrespective of presence/absence of edge detection in the edge detection circuit 42.

(52) The paragraph from page 51, line 15 to page 51, line 20 has been amended as follows:

As a result, in (2) ~~Continuously~~ Continuous Mode, the positional data indicative of the edge timing is continuously output with a timing of the strobes of the delay circuit 22 irrespective of presence/absence of edge detection of the positional data, stored in each of the registers 41a to 41n, and output.

(53) The paragraph from page 51, line 25 to page 52, line 1 has been amended as follows:

Subsequently, outputting the average value output from the average value calculation circuit 44 ((1) Smoothing Mode) or outputting the positional data output from the register 41a on the forefront stage as it is ((2) Sampling Mode) is switched by switching ~~of~~ the average value changeover switch

45, and thus either one of the positional data is output to the timing correction circuit 46.

(54) The paragraph from page 55, line 16 to page 55, line 26 has been amended as follows:

In the time interpolator 20 of each source synchronous circuit, the system clock and the output data output from the device under test 1 are obtained as level data in which the number of bits is "4" with a frequency timing of the internal clock of the device under test 1. Moreover, SDR: Rise Edge is selected in the edge selector 23 of the time interpolator 20, the edge changeover switch 43 is set to (1) ~~Continuously~~ Continuous Mode, the average value changeover switch 46 is set to (1) Smoothing Mode, and the mode changeover switch 47 is set to (2) Hold Edge (see FIG. 1) in the digital filter 40.

(55) The paragraph from page 56, line 16 to page 56, line 23 has been amended as follows:

In the digital filter 40, (2) ~~Continuously~~ Continuous Mode is selected by the edge changeover switch 43. When an edge of positional data is detected, this positional data is output. When an edge is not detected, positional data in a previous cycle is output. The positional data (e.g., "10") indicative of the bit number "3" is sequentially stored in and output from the registers 41a to 41n starting from the register 41a on the forefront stage.

(56) The paragraph from page 57, line 14 to page 57, line 20 has been amended as follows:

As a result, in the selector 30 on the output data side, data of the input terminal corresponding to "10" (bit number "3") indicated by the recovery clock is selected (struck out) with the cycle of the internal clock while using the recovery clock as a selection signal as shown in FIG. 2, and ~~predetermined~~ the retrieved data "H" or "L" is thereby output from the selector 30.

(57) The paragraph from page 60, line 1 to page 60, line 11 has been amended as follows:

A description will now be given as to an embodiment in which the mode changeover switch 47 of the digital filter 40 is switched to Direct Edge in the test apparatus according to this embodiment with reference to ~~FIGS. 5~~ FIGS. 5(a) and 5(b). ~~FIGS. 5~~ FIGS. 5(a) and 5(b) are signal diagrams in case of obtaining output data with an edge timing of the system clock when the mode changeover switch 47 of the digital filter 40 is switched to Direct Edge, in which FIG. 5(a) shows an example of obtaining data with a rise edge timing of the clock and FIG. 5(b) shows an example of obtaining data with both rise and fall edges.

(58) The paragraph from page 60, line 12 to page 60, line 19 has been amended as follows:

In the test apparatus according to this embodiment, by switching the mode changeover switch 47 to Direct Edge, positional data obtained by the encoder 28 on the clock side is input to the selector 30 on the output side, and it is possible to conduct a test of a device from which output data is output with a timing synchronized with the system clock of the device like a regular SDR or DDR type device.

(59) The paragraph from page 62, line 1 to page 62, line 9 has been amended as follows:

It is to be noted that the test can be of course performed to the above-described regular SDR or DDR type device by using the recovery clock obtained by the digital filter 40. By using the recovery clock obtained by the digital filter 40 with respect to the DDR type device, data can be acquired only by using the accurate edge timing in case of testing the device ~~with~~ whose accuracy with respect to one of the rise edge and the fall edge of the system clock ~~being poor~~ is low, for example.

(60) The paragraph from page 63, line 26 to page 64, line 14 has been amended as follows:

In the time interpolator 20 on the clock side, the level data and the positional data indicative of the edge timing of the clock can be obtained. However, as described above, when the device under test 1 is an ODR type device which outputs data with timings of both the rise edge and the fall edge of

the internal clock having a frequency which is fourfold of that of the system clock, the rise edge (or the fall edge) is detected only once in eight times even if the timing of the rise edge (or the fall edge) of the system clock having a 1/4 frequency ~~is obtained~~ of the internal clock is input to the synchronous circuit 10a. Furthermore, a signal change point (rise or fall edge) cannot be detected in any other cycle, and the timing edge of the internal clock having a fourfold frequency is thereby obtained only once in eight times. Moreover, the clock signal output from the device under test 1 has jitters, and the edge timing indicated by the positional data of the clock does not ~~become a~~ show an accurate timing which is adequate as a timing signal used to obtain test data in some cases.

(61) The paragraph from page 65, line 17 to page 65, line 19 has been amended as follows:

A second embodiment of the semiconductor test apparatus according to the present invention will now be described with reference to ~~FIG. 7~~ FIG. 8.

(62) The paragraph from page 65, line 20 to page 65, line 28 has been amended as follows:

~~FIG. 7~~ FIG. 8 is a block diagram showing a structure of a semiconductor test apparatus according to the second embodiment of the present invention. As shown in the drawing, the semiconductor test apparatus according to this embodiment

is a modified embodiment of the above-described first embodiment, and a jitter detection circuit 60 is further provided to the source synchronous circuit (clock recovery circuit) 10a on the clock side in the first embodiment.

(63) The paragraph from page 68, line 23 to page 69, line 1 has been amended as follows:

In this embodiment, as shown in ~~FIG. 7~~ <u>FIG. 8</u>, a judgment changeover switch 64 is provided to an input portion to the fail analysis memory or the like, and a mode to store the acceptability judgment result in the pattern comparator 12 ((1) Data Exp Mode shown in ~~FIG. 7~~ <u>FIG. 8</u>) can be switched to/from a mode to store the judgment result of the comparison judgment circuit 63 ((2) Jitter Fail Mode shown in the same drawing) as to the fail analysis memory or the like.

(64) The paragraph from page 69, line 2 to page 69, line 13 has been amended as follows:

As described above, according to the semiconductor test apparatus of this embodiment, by providing the jitter detection circuit 60 which receives a plurality of recovery clocks, a phase difference between the recovery clocks can be detected by applying the subtraction processing to the positional data indicative of edge timings of the respective recovery clocks. Further, ~~a~~ distribution of the phase ~~difference~~ <u>differences</u> detected by the jitter detection circuit 60 can be obtained, and it can be output as

distribution data showing irregularities or spread of the phase differences.

(65) The paragraph from page 70, line 30 to page 71, line 10 has been amended as follows:

That is, the clock recovery circuit constituting the semiconductor test apparatus according to the present invention can be obtained by combinations of any circuits, apparatus and others as long as it comprises the time interpolator which acquires output data of the device under test as time-series level data and the digital filter which can obtain and output a recovery clock based on the level data acquired by the time interpolator, and an application, an object and others as the semiconductor test apparatus are not ~~restricted in particular~~ limited to particular examples.

(66) The paragraph from page 71, line 12 to page 71, line 12 has been amended as follows:

~~Industrial Applicability~~

(67) The paragraph from page 71, line 13 to page 71, line 20 has been amended as follows:

As described above, according to the semiconductor test apparatus of the present invention, by providing the time interpolator and the digital filter, a system clock output from the device under test can be acquired, and a recovery clock having a frequency of an internal clock faster than ~~a~~

the system clock can be obtained with a timing of a rise edge or a fall edge of the system clock.